Abstract

Disclosed is a video data re-clocking scheme for use in highly integrated system circuits to overcome the problem of beat patterns. These type of circuits contain many subsystem blocks, and each of those blocks may use different clock frequencies. Due to implementation constraints, clock interferences from nearby blocks are unavoidable. In a video display sub-system, these interferences produce beat patterns that substantially degrade video quality. One disclosed embodiment of the invention employs re-clocking flip-flops to re-time the input signals feeding the video Red/Green/Blue Digital-to-Analog converters (RGB DACs) such that data edge jitters due to interference are removed. The resulting picture quality is free of beat patterns.

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